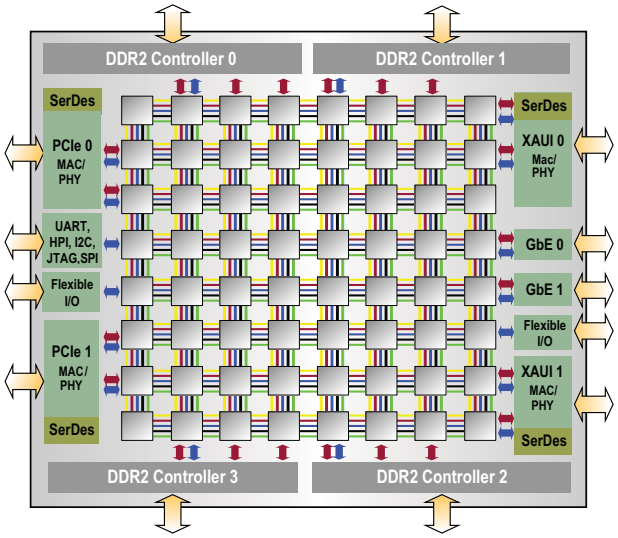
TILERA™
EMBEDDING MULTICORE

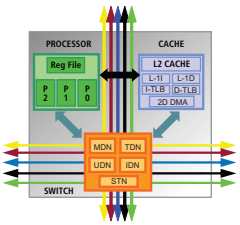
TILE64™ Processor

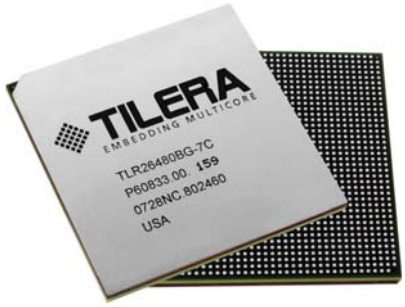
Product Brief

Overview

The TILE64™ family of multicore processors delivers immense compute performance to drive the latest generation of embedded applications. This revolutionary processor features 64 identical processor cores (tiles) interconnected with Tilera's iMesh™ on-chip network. Each tile is a complete full-featured processor, including integrated L1 & L2 cache and a non-blocking switch that connects the tile into the mesh. This means that each tile can independently run a full operating system, or multiple tiles taken together can run a multi-processing OS like SMP Linux.







The TILE64 processor family slashes board real estate and system cost by integrating a complete set of memory and I/O controllers, therefore eliminating the need for an external North Bridge or South Bridge. It delivers scalable performance, power efficiency and low processing latency in an extremely compact footprint.

The TILE64 Processor is programmable in ANSI standard C, enabling developers to leverage their existing software investment. Tiles can be grouped into clusters to apply the appropriate amount of horsepower to each application. Since multiple operating system instances can be run on the TILE64 simultaneously, it can replace multiple CPU subsystems for both the data plane and control plane.

Combining multiple C-programmable processor tiles with the iMesh multicore technology enables the TILE64 processor to achieve the performance of a fixed function ASIC or FPGA in a powerful software-programmable solution.

Product Differentiators

	Features	Enables
Massively Scalable Performance	• 8 X 8 grid of identical, general purpose processor cores (tiles) • 3-way VLIW pipeline for instruction level parallelism • 5 Mbytes of on-chip Cache • 192 billion operations per second (32-bit) • 27 Tbps of on-chip mesh interconnect enables linear application scaling • Up to 50 Gbps of I/O bandwidth	• 10 Gbps Snort® processing • 20+ Gbps iptables (firewall) • 20+ Gbps nProbe • 16 X 16 SAD at 540 MBlocks/s • H.264 HD video encode for two streams of 720p @ 30 Fps
Power Efficiency	• 600MHz - 1GHz operating frequency • 170 - 300mW per core • Idle Tiles can be put into low-power sleep mode • Power efficient inter tile communications	• Highest performance per watt • Simple thermal management & power supply design • Lower operating cost
Integrated Solution	• Four DDR2 memory controllers with optional ECC • Two 10GbE XAUI configurable MAC or PHY interfaces • Two 4-lane 10Gbps PCI-e MAC or PHY interfaces • Two GbE MAC interfaces • Flexible I/O interface	• Reduces BOM cost - standard interfaces included on-chip • Dramatically reduced board real estate • Direct interface to leading L2-L3 switch vendors
Multicore Development Environment	• ANSI standard C compiler • Advanced profiling and debugging designed for multicore programming • Supports SMP Linux with 2.6 kernel • iLib API's for efficient inter-tile communication	• Run off-the-shelf C programs • Reduce debug and optimization time • Faster time to production code • Standard multicore communication mechanisms

Targeted Applications

The TILE64 family of processors has both the flexibility and performance to support a wide range of compute-intensive applications, including advanced networking, digital video, and telecom. Because it is a general purpose, MIMD multicore processor, it can run multiple operating systems and applications simultaneously. For example, it can perform 10Gbps of TCP offload (TOE) along with multiple streams of video transcoding. Virtual memory support and Tilera's Multicore Hardwall™ technology provides kernel-level protection related to both shared memory and user-level streaming and messaging.

Advanced Networking Products. The TILE64 processor is ideally suited to intelligent network services such as Unified Threat Management (UTM), L4-7 deep packet inspection, or Quality of Service (QoS) provisioning. The impressive compute performance together with a complete integrated networking I/O subsystem makes the TILE64 a powerful single-chip communications processor.

Digital Multimedia Products. The TILE64 processor also excels at digital video processing, easily taking the place of multiple DSPs to perform video encoding, transcoding, video analytics, or other digital video manipulation. In addition, the control plane and any required networking capability can be handled by the same TILE64 device.

Available in multiple configurations with a variety of I/O interfaces and DDR2 memory compliments, the TILE64 processor family offers devices positioned across a range of applications.

Development Environment

Tilera's Multicore Development Environment™ (MDE) is a complete standards-based multicore programming solution that enables developers to take full advantage of the parallel processing potential of the Tile Processor™ architecture.

Powerful innovations allow the developer to take a Gentle Slope Programming™ approach to multicore software development. Leveraging Open Source software and the developer's existing software code base, impressive results can be achieved in an extremely short period of time. Then, as developers become more familiar with large-scale multicore, they can take advantage of the enhanced tools and libraries offered in the MDE to optimize performance further.

Tilera's MDE includes:

- Standard Eclipse-based IDE
- ANSI standard C compiler
- Multi-tile cycle-accurate simulator
- Whole chip debug and performance analysis
- Complete SMP Linux support
- iLIB library for efficient inter-communication
- PCIe Hardware development platform
- Linux and Windows host environments

Scalable Processing and Ease of Use for Embedded Application Developers

The TILE64 Processor addresses application developers' needs for scalable multiprocessor performance, performance per watt, and ease of development. The Tile Processor's on-chip iMesh network, the distributed cache architecture, and the industry-standard development tools combine to provide a solution uniquely suited to today's networking and multimedia applications.

Ordering Information:

Part Number	Number of Tiles	Memory	I/O Interfaces	Frequency	Operating Temperature
TLR26420 BG-xC	64	2 DDR2	2 PCI-e , 2 GbE	600 MHz - 900 MHz	Commercial
TLR26420 BG-xI					Industrial
TLR26440 BG-xC	64	4 DDR2	1 XAUI, 1 PCI-e, 2 GbE	600 MHz - 900 MHz	Commercial
TLR26440 BG-xI					Industrial
TLR26480 BG-xC	64	4 DDR2	2 XAUI, 2 PCI-e, 2 GbE	600 MHz - 900 MHz	Commercial
TLR26480 BG-xI					Industrial

x = Frequency code: 6=600MHz, 7=750MHZ, 9=900MHz

For more information on Tilera products, visit www.tilera.com

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Rev 1

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